In the Claims

Cancel claims 39 and amend 41, 42, 43, 45, 46, and 51. The claims are as follows:

1. – 40. (CANCELLED)

41. (CURRENTLY AMENDED) A method of fabricating a shadow mask, comprising the steps of:

a) providing an array of holes in the shadow mask corresponding to contacts on an array of chips on a wafer, said array of chips including perimeter chips extending along a periphery of the wafer; and

b) providing a first set of additional ~~dummy~~ holes in the shadow mask located adjacent holes corresponding to most of said perimeter chips wherein said first set of additional ~~dummy~~ holes are for improving contact processing of said perimeter chips wherein said first set of additional ~~dummy~~ holes are omitted in saw blade lanes and in a ring shaped exclusion zone in an area of the shadow mask beyond said perimeter chips ~~and beyond said dummy holes~~.

42. (CURRENTLY AMENDED) The method of fabricating a shadow mask as recited in claim 41, further comprising the step of inspecting the shadow mask using first set of additional ~~dummy~~ holes along an edge of a dicing lane to align the shadow mask to an inspection device.

43. (CURRENTLY AMENDED) A method of fabricating a shadow mask, comprising the steps of: ~~—~~

a) providing an array of holes in the shadow mask corresponding to contacts on an array of chips on a wafer, said array of chips including perimeter chips extending along a periphery of the wafer;

b) providing a first set of additional holes in the shadow mask located adjacent holes corresponding to most of said perimeter chips wherein said first set of additional holes are for improving contact processing of said perimeter chips wherein said first set of additional holes are omitted in saw blade lanes and in a ring shaped exclusion zone in an area of the shadow mask beyond said perimeter chips, and

~~The method of fabricating a shadow mask as recited in claim 41, further comprising the step of~~ c) inspecting the shadow mask using a pattern of a second set of additional holes, said second set of additional holes located beyond holes corresponding to said perimeter chips, said second set of additional holes for aligning the shadow mask to an inspection device, wherein said pattern of second set of additional holes does not print on the wafer.

44. (CURRENTLY AMENDED) The method of fabricating a shadow mask as recited in claim 43, wherein said pattern of the second set of additional holes is located so that it will be covered by a guard ring.

45. (CURRENTLY AMENDED) The method of fabricating a shadow mask as recited in claim 43, further comprising the step of inspecting the shadow mask using a covering for said second set of additional ~~dummy~~ holes.

46. (CURRENTLY AMENDED) The method of fabricating a shadow mask as recited in claim 45 ~~41~~, wherein said covering for said secont set of additional ~~dummy~~ holes is a ring having an inside edge corresponding to outside edges of perimeter chips.

47. – 50. (CANCELLED).

51. (CURRENTLY AMMENDED) A method of fabricating a shadow mask, comprising the steps of:

a) providing an array of holes in the shadow mask corresponding to contacts on an array of chips on a wafer, said array of chips including perimeter chips extending along a periphery of the wafer; and

b) providing a first set of additional ~~dummy~~ holes in the shadow mask located adjacent holes corresponding to most of said perimeter chips wherein said first set of additional ~~dummy~~ holes are for improving contact processing of said perimeter chips wherein said first set of additional ~~dummy~~ holes are omitted in a ring shaped exclusion zone in an area of the shadow mask beyond said perimeter chips ~~and beyond said dummy holes~~.

REMARKS